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09/988,208	11/19/2001	Kazuyuki Ohhashi	P21699	8111

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EXAMINER	
AGHDAM, FRESHTEH N	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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DETAILED ACTION

Applicant's Argument(s):

Regarding claims 25, 26, 28, and 33, pages 7-13, the applicant argues that the claimed subject matter "amplitude adjustment after sign inversion and before phase offsetter" because:

(1) by performing amplitude multiplication after the first offset processing performed and before the second offset processing is performed, it is possible to reduce an amount of calculation in comparison to the prior art shown in figure 4B.

(2) the applicant made the assumption that the combination of Sato and the instant application's disclosed prior art would result in the drawing shown on page 8.

(3) figure 1 of Sato already shows power amplifier 106 after the QPSK spreading circuit 102,so there is no reason to replace power amplifier 106 in Sato with amplifier multiplier 406 in the applicant's disclosed prior art.

(4) regarding claims 28 and 33, the applicant argues "SATO as modified by Applicant's disclosed prior art would not result in the combinations of claims 28 and 33, including controlling the second phase offsetting based on a signal from a remote source."

Examiner's Response:

Regarding the argument set forth above, the examiner **strongly disagrees** with the applicant for at least three reasons, which are as follows:

(1) the **examiner is still unclear as to why the inputs to the amplitude multiplier of the admitted prior art (fig. 4B) is the same as the inputs to the amplitude multiplier of figure 4A *(this issue raised by the examiner has not been responded by the applicant yet)***, and as it was stated in the previous office action, Sato teaches obtaining the first phase offset of multiple of 90° using a sign inverter (means 201) and providing the second phase offset smaller than 90° using a phase offset calculation circuit to a signal output from the sign inverter (means 202). The instant application's disclosed prior art discloses adjusting the amplitude of the signal to be inputted to the phase offset calculation circuit (fig. 4B means 406 and 407) since the inputs (SRI, SRQ) to the amplitude multiplier 406 of figure 4B (labeled as prior art) are the same as the input signals (SRI, SRQ), which are the same as the intermediate components to the amplitude multiplier of figure 4A (disclosure of the present invention), therefore, it seems that the difference between the present invention and the prior art is the way the signals SRI and SRQ are obtained not the amplitude adjustment (also see the specification, pg. 3) and, in fact, the amplitude adjuster is placed between the first phase offset processing and the second phase offset processing.

(2) **in addition, one of ordinary skill in the art would recognize that amplitude adjustment and phase adjustment are necessary in the IMT2000-compliant W-CDMA (pg. 1-2) and unlike the applicant's assertion that placing the amplitude adjustment makes it possible to reduce an amount of calculation in comparison to the prior art shown in figure 4B (remarks, pages 5-6), according to the original disclosure of the invention, the invention is directed to phase offset**

calculation, and in particular to using two phase offset circuitries, wherein the first one is a sign inventor to obtain a first phase offset of multiple 90 degrees and the second one provides a second phase offset of smaller than 90 degrees and this two-stage configuration simplifies the circuit (e.g. reducing an amount of calculation) and reduces power consumption of the circuit (spec. pg. 1, lines 5-9; pg. 4, lines 1-28 and particularly lines 20-22; pg. 5, lines 1-5; pg. 10, lines 24-28). Therefore, the placement of the amplitude adjuster does not affect the phase adjustment, so, **it would enable one of ordinary skill in the art to place the amplitude adjuster between the sign inverter and the phase offset calculation circuit, before both the sign inverter and the phase offset calculation circuit, or after the sign inverter and the phase offset calculation circuit as long as the amplitude adjuster complies with the IMT2000 W-CDMA requirements (e.g. serves its purpose).**

(3) the instant application's disclosed prior art teaches a transmission controller that provides control information from a remote source to the phase offsetting circuit **(e.g. the second phase offsetting; Fig. 4, Pg. 1, Lines 16-28; Pg. 2, Lines 1-5)**. It would have been obvious to one of ordinary skill in the art to control the operation of the phase offsetting circuitry based on a control signal received from a remote source as taught by the instant application's disclosed prior art in order to improve the level of a reception signal and clearly distinguish between interference signals from other mobile stations and the original reception signal (Pg. 2, Lines 1-5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRESHTEH N. AGHDAM whose telephone number is (571)272-6037. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/F. N. A./

Examiner, Art Unit 2611

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611